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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
CHEN, KIN CHAN

ART UNIT	PAPER NUMBER
1765	6

DATE MAILED: 09/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

TC-6

Office Action Summary	Application No. 09/867,563	Applicant(s) SHIH, TSU	
	Examiner Kin-Chan Chen	Art Unit 1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-23 and 25-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-23 and 25-27* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Objections

1. Claim 10 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 10 recites the removing of fill material by etching which is broader than CMP process recited in claim 1.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1,2, 4,5,7and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,042,999) in view of Wang et al. (US 6,057,239).

In a method for forming a dual damascene structure and protecting the substrate from damage caused by multiple etchings, Lin teaches (col. 4, line 41 through col. 6, line 30) providing a substrate having first and second insulative layers, separated from each other by an intervening etch-stop layer formed thereon (Fig. 2a); forming a hole

opening through the first and second insulative layers (Fig. 2b); forming a fill material over the substrate, including in the hole opening (Fig. 2C); removing any excess fill material over the hole opening (Fig. 2d); forming a trench opening in the second insulative layer over the hole opening in the first insulative layer, thus completing the forming of the dual damascene structure on the substrate (Fig. 2e); removing the fill material from the hole opening (Fig.2f); depositing metal in the dual damascene structure and removing excess metal to complete the forming of the dual damascene (Figs 2g and 2h).

Lin teaches fill material may be ARC, BARC, or organic BARC (col. 5, lines 36-38, 53-56). Therefore, it includes I-line PR (photo-resist) and spin-on organic dielectric such as SiLK or FLARE because they are well-known ARC. Wang is relied on to teach this well-known feature. In a method of dual damascene process using sacrificial spin-on materials, Wang teaches a sacrificial layer of spin-on material, an anti-reflective coating (ARC) material such as **BARLi (I-line photo-resist)** or FLARE (so-called spin-on organic oxide in instant claim 9) may be used for protecting the contact hole profile during the damascene etch process (col. 3, lines 9-14; col.1, lines 10-11). Hence, it would have been obvious to one with ordinary skill in the art to use said material as taught by Wang in the process of Lin in order to protect the contact hole profile during the damascene etch process.

Lin and Wang teach that performing the above process steps would protect the surface of the substrate from damage. The instant claims differ from Lin and Wang by specifying eliminating (without) volcano effect in dual damascene, however, since Lin

and Wang teach the method claimed, the claimed property and function (such as eliminating volcano effect) is considered to be inherent.

Claim 1 differs from the combined prior art by specifying removing the excess fill material by chemical mechanical polishing (CMP). However, it is a **conventional process** in the art of semiconductor device fabrication to remove the excess fill material by chemical mechanical polishing. Hence, it would have been obvious to one with ordinary skill in the art to modify the combined prior art by using the said conventional CMP to remove the excess fill material in order to provide their art recognized advantages and produce an expected result. The cited references below are only as **evidences** of the prior **comventional** process (CMP) statement, see Rodriguez et al. (US 5,821,160, col. 8, lines 54-56); Skee et al. (US 5,989,353; col. 3, lines 20-21); Tu et al. (US 6,309,957; col. 3, lines 31-32, col. 4, lines 42-45); Badih (FSPT; pages 547, 565-566), all in the record.

The use of conventional materials to perform their known functions in a conventional process is obvious. In re Raner 134 USPQ 343.

As to dependent claim 2, Lin teaches silicon substrate (col. 4, line 42).

As to dependent claim 4, Lin teaches the thickness which overlaps the claimed range (col.5, line 9).

As to dependent claim 5, Lin teaches silicon nitride (col. 5, lines 10-11).

As to dependent claim 7, Lin teaches the thickness which overlaps the claimed range (col.5, line 9).

As to dependent claim 10, Lin teaches that the excess fill material may be removed by etching (col. 5, lines 62-67).

As to dependent claims 11 and 13, Lin teaches that metal may comprises copper (col. 7, lines 25-27), and excess metal may be removed by chemical mechanical polishing (col. 7, lines 25-30).

Lin does not disclose the metal thickness used in his dual damascene process. Dependent claim 12 differs from Lin by specifying the thickness of metal may be between 1000 to 15000 A. However, the thickness of deposited metal is merely a matter of choice of design depending on product requirement. Hence, it would have been obvious to one with ordinary skill in the art to deposit the suitable thickness for the metal in order to meet the product requirement and produce an expected result.

4. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,042,999) and Wang et al. (US 6,057,239) as applied to claim 1 above, and further in view of Tsai et al. (US 6,326,296 B1).

The discussion of Lin and Wang from above is repeated here.

As to dependent claims 3 and 6, Lin teaches that the dielectric layers (so-called the first insulative layer in instant claim 3; the second insulative layer in instant claim 6) may be materials, which are known in the art and not limited to silicon oxide materials. Therefore, the materials may include low-k dielectric because it is one of the most popular dielectric materials used in the art of semiconductor device fabrication. Tsai is only relied on to show this low-k dielectric material (col. 5, lines 38-40). In addition, it is well known in the art that low-k dielectric material typically has a dielectric constant

between about 2.5 to 3.5. Because low-k dielectric material is a well-known feature in the art, hence, it would be obvious to one skilled in the art to modify Lin and Wang by using said material as disclosed by Tsai in order to provide their art recognized advantages and thus produce an expected result.

5. Claims 14-16, 18, 19, 21-23 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,042,999) in view of admitted prior art and Wang et al. (US 6,057,239).

In a method for forming a dual damascene structure and protecting the substrate from damage caused by multiple etchings, Lin teaches (col. 4, line 41 through col. 6, line 30) forming a first insulative layer on the substrate, forming an etch-stop layer over the first insulative layer, and forming a second insulative layer over the etch-stop layer; forming a first photoresist layer over the second insulative layer and patterning the photoresist to form a first photoresist mask having a hole pattern(Fig. 2a); etching the first and second insulative layer including the etch-stop layer through the hole pattern to form a hole reaching the substrate and removing the first photoresist mask(Fig. 2b); forming a fill material over the substrate, including in the hole opening(Fig. 2C); removing any excess fill material over the hole opening,(Fig. 2d); forming a second photoresist layer over the substrate including the hole opening and patterning the second photoresist to form a second photoresist mask having a trench pattern (Fig. 2C); etching the second insulative layer through the trench pattern in the second photoresist mask to form a trench in the second insulative layer, thus completing the forming of the

dual damascene structure in the substrate and removing the second photoresist mask(Fig. 2e); removing the fill material from the hole opening (Fig.2f); depositing metal in the dual damascene structure and removing excess metal to complete the forming of the dual damascene (Figs 2g and 2h).

Lin teaches that performing the above process steps would protect the surface of the substrate from damage. The instant claims differ from Lin by specifying eliminating (without) volcano effect in dual damascene, however, since Lin teaches the method claimed, the claimed property and function (such as eliminating volcano effect) is considered to be inherent.

Lin teaches that substrate may include substructure with metal layers (col. 4, lines 49-50). Therefore, it may include a metal layer with passivation layer formed thereon because it is a common substructure in the art of semiconductor device fabrication. The admitted prior art is relied on to teach this well-known substructure. The admitted prior art teaches that the substrate is provided with metal layer and barrier layer (so-called passivation layer in the instant claim 14). The metal layer may be copper (instant claim 16). See the specification, page 4, lines 13-16. Hence, it would have been obvious to one with ordinary skill in the art to modify Lin by using this well-known substructure as taught by admitted prior art in order to provide their art recognized advantages and produce an expected result.

Lin teaches fill material may be ARC, BARC, or organic BARC (col. 5, lines 36-38, 53-56). Therefore, it includes I-line PR (photo-resist) and spin-on organic dielectric such as SiLK or FLARE because they are well-known ARC. Wang is relied on to teach

this well-known feature. In a method of dual damascene process using sacrificial spin-on materials, Wang teaches a sacrificial layer of spin-on material, an anti-reflective coating (ARC) material such as BARLi (I-line photo-resist) or FLARE (col. 3, lines 9-14), may be used for protecting the contact hole profile during the damascene etch process (col.1, lines 10-11). Hence, it would have been obvious to one with ordinary skill in the art to use said material as taught by Wang in the process of Lin and admitted prior in order to protect the contact hole profile during the damascene etch process.

Claim 14 differs from Lin and admitted prior art by specifying removing the excess fill material by chemical mechanical polishing (CMP). However, it is a **conventional process** in the art of semiconductor device fabrication to remove the excess fill material by chemical mechanical polishing. Hence, it would have been obvious to one with ordinary skill in the art to modify the combined prior art by using the said conventional CMP to remove the excess fill material in order to provide their art recognized advantages and produce an expected result. The cited references below are only as **evidences** of the prior **comventional** process (CMP) statement, see Rodriguez et al. (US 5,821,160, col. 8, lines 54-56); Skee et al. (US 5,989,353; col. 3, lines 20-21); Tu et al. (US 6,309,957; col. 3, lines 31-32, col. 4, lines 42-45); Badih (FSPT; pages 547 and 565-566), all in the record.

As to dependent claim 15, Lin teaches silicon substrate (col. 4, line 42).

As to dependent claim 16, the admitted prior art is relied on for the same reasons as stated, supra.

As to dependent claim 18, Lin teaches the thickness which overlaps the claimed range (col.5, line 9).

As to dependent claim 19, Lin teaches silicon nitride (col. 5, lines 10-11).

As to dependent claim 21, Lin teaches the thickness which overlaps the claimed range (col.5, line 9).

As to dependent claim 25, Lin teaches that metal may comprises copper (col. 7, lines 25-27).

As to dependent claim 26, Lin and admitted prior art do not disclose the second metal thickness used in his dual damascene process. Dependent claim 26 differs from Lin and admitted prior art by specifying the thickness of the second metal may be between 1000 to 15000 A. However, the thickness of deposited metal is merely a matter of choice of design depending on product requirement. Hence, it would have been obvious to one with ordinary skill in the art to deposit the suitable thickness for the metal in order to meet the product requirement and produce an expected result.

As to dependent claim 27, Lin teaches excess metal may be removed by chemical mechanical polishing (col. 7, lines 25-30).

6. Claims 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,042,999), admitted prior art and Wang et al. (US 6,057,239) as applied to claim 14 above, and further in view of Tsai et al. (US 6,326,296 B1).

The discussion of Lin, admitted prior art and Wang from above is repeated here.

Lin teaches that the dielectric layers (so-called the first insulative layer in instant claim 17; the second insulative layer in instant claim 20) may be materials, which are

known in the art and not limited to silicon oxide materials. Therefore, materials may include low-k dielectric because it is one of the most popular dielectric materials used in the art of semiconductor device fabrication. Tsai is only relied on to show this low-k dielectric material as an insulating layer(col. 5, lines 38-40). In addition, it is well known in the art that low-k dielectric material typically has a dielectric constant between about 2.5 to 3.5. Because low-k dielectric material is a well-known feature in the art, hence, it would be obvious to one skilled in the art to modify Lin,admitted prior art and Wang by using said material as disclosed by Tsai in order to provide their art recognized advantages and thus produce an expected result.

Response to Arguments

7. Applicant's arguments filed on August 19, 2002 have been fully considered but they are not persuasive.

In response to applicant's argument that Lin does not use I-line photoresist as a fill material, as stated in the office action, Lin teaches fill material may be ARC, BARC, or organic BARC (col. 5, lines 36-38, 53-56). Therefore, it includes I-line PR (photo-resist) and spin-on organic dielectric such as SiLK or FLARE because they are well-known ARC. Wang is relied on to teach this well-known feature. Wang teaches a sacrificial layer of spin-on material, an anti-reflective coating (ARC) material such as **BARLi (I-line photo-resist)** may be used for protecting the contact hole profile during the damascene etch process.

One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. In re Merk &Co., Inc., 800F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). (our ref. Only ..MPEP 2145 IV.)

In response to applicant's argument that Lin does not use chemical mechanical polishing (CMP) to remove the excess fill material, as stated in the office action, it is a **conventional process** in the art of semiconductor device fabrication to remove the excess fill material by chemical mechanical polishing. The cited references (in the record) are as **evidences** of the **comventional** process (CMP). The use of conventional materials to perform their known functions in a conventional process is obvious. In re Raner 134 USPQ 343.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Rodriguez et al. (US 5,821,160, col. 8, lines 54-56) teach All of conductive layers and dielectrics may be subjected to CMP at different stages of manufacturing; Badih, Fundamentals of semiconductor processing technologies (FSPT), pages 547 and 565-566, teaches that dielectric (insulators) materials include organic materials. Skee et al. (US 5,989,353; col. 3, lines 20-21) teach photoresist (so-called I-line photoresist in the instant claims) is a polymeric organic material; Tu et al. (cited in previous PTO-892, US 6,309,957; col. 3, lines 31-32, col. 4, lines 42-45) teach low-k material such as organic material may be planarized by CMP.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kin-Chan Chen whose telephone number is (703) 305-0222. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on (703) 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9310 for regular communications and (703) 872-9311 for After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-2934.

K-C C
September 3, 2002.

BENJAMIN L. UTECH
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